Formation and Characterization of Defects in 2-Step Processing of Cu(In, Ga)Se Solar Cells

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ABSTRACT

Using 2-step all-solid-state processing we have achieved good electronic properties in CIGS solar cells for band gaps below 1 eV. As we add Ga to increase the band gap, there is deterioration in properties resulting in poorer device performance. We have used a combination of advanced measurement techniques and simulations to understand the Ga incorporation mechanisms that control fundamental properties. Photocapacitance techniques are particularly sensitive to defects and greatly enrich the experimental data base. To properly model observed behavior we find that improperly bonded Ga produces both acceptors and acceptor defects. These appear to be linked, and the defect is 0.29 eV from the valence band edge which ties it to theoretical calculations of Cu vacancies. Through the insights gained from these studies we have improved our Ga incorporation procedures and have realized improvements in device performance.

1. Introduction

The understanding and control of defects is the key to further development of CIGS solar cells. Development in this case refers not just to advancements in laboratory cell efficiency, but to commercialization issues such as manufacturability and stability. There are ongoing efforts to understand the fundamental defect structure of these materials such as those of the NREL theory group. While this understanding is still being developed, those of us who run processing efforts must work within the confines of present understanding to continue making progress. Since we are particularly concerned with manufacturability, we must not only understand what the material is and can be, but also how to make it that way within the stringent cost constraints of a manufacturing line. We have had good success in using manufacturing–friendly 2-step processing to make low band gap devices. However, higher efficiencies can be achieved in devices with a higher energy gap. The highest efficiency devices to date have a band gap in the 1.1 –1.2 eV range. These are typically made by coevaporation, and the performance levels of devices made by the 2-step process, especially using solid-source selenization, are lower. The central issue seems to be the effective incorporation of Ga. In raising the energy gap, Ga also contributes additional states that affect performance. The nature and magnitude of these states is a function of the processing conditions. Coevaporation does the best job of placing Ga where it is needed and with the right attributes. We need to learn how to do this with 2-step processing. In this paper we report on progress made toward this objective.

2. Results and Discussion

In devices with Eg below 1 eV we routinely achieve Jsc's in excess of 40 mA/cm^2 , and by tuning the surface properties have combined this with Voc's in excess of 500 mV. These devices have only trace amounts of Ga in the space charge layer with the bulk of the Ga deposited(~10% Ga/(In + Ga)) going to the rear of the device. As we adjust our processing conditions to cause Ga to bond at alloy levels in the space charge region, we typically see a deterioration of electronic properties. The effects on Jsc and Voc for a series of runs covering the range 1.03   Eg   1.15 are seen in figures 1 and 2. Jsc's are from integrated QE spectral response using NREL calibrated references. The curve labeled "ideal" for Jsc is a simulation of Jsc behavior if only band gap changes occur
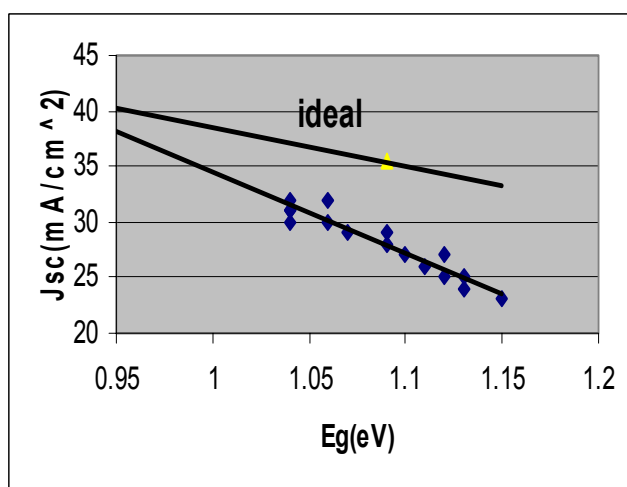

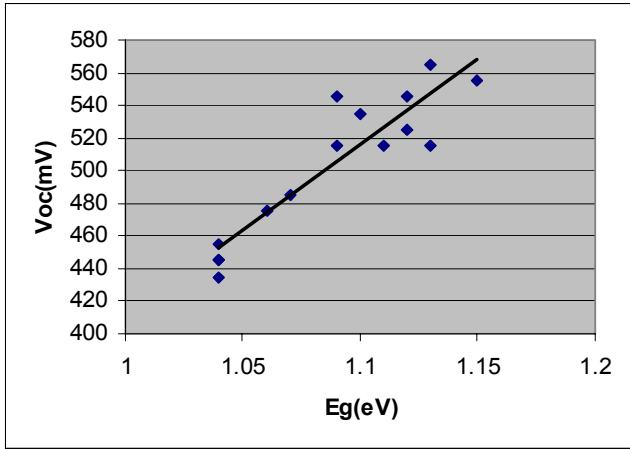**Figure 1. Jsc vs. Eg for a series of CIGS runs(   ), and ideal Jsc vs. Eg from simulation.**

Figure 2. Voc vs. Eg for the devices of figure 1.

and there are no other losses. Clearly under these run conditions as soon as we raise the band gap we introduce mechanisms that result in current collection losses. Analysis of QE spectra indicates that the losses are due to both red collection and down shifting of the overall spectrum. Although Voc values are downshifted as well due to an additional loss factor, they do track Eg on a one-to-one basis. The scatter in figure 2 is a manifestation of the other mechanisms controlling Voc.

To study these issues more closely we look at data from the 25 devices from a single run. Our deposition configuration produces compositional gradients that are very useful for monitoring subtle changes in electronic properties. In figure 3 we show data for the Cu/In gradient of a single run. Each data point is the average of 5 devices with the same Cu/In ratio. The ratio changes from about 1.0 on the Cu side(position 1) to 0.95 on the In side(position 5). Over this range the band gap increases from 1.06 to 1.12 eV. An In rich environment fosters Ga alloying. The data also shows the opposing behavior of Jsc and Voc characteristic of the set of runs discussed above. The advantage here with data from a single run is that concern with unknown run-to-run parameters is eliminated. Another key piece of data in the figure is the dark capacitance. As can be seen, it increases along with Ga alloying as the Cu/In ratio is decreased. This in part accounts for some of the additional Jsc loss beyond band gap changes. Furthermore, it indicates an increase in net acceptor concentration with increasing Ga incorporation. To pull this all together we turn to AMPS simulations. Simulation of the data in figure 3 along with additional QE data severely constrains the options one has for a device model. Getting Voc and Jsc to go in opposite directions to fit the above data while the acceptor concentration was increasing forced the realization that Ga was introducing a complex acceptor defect that could not be simulated by a single entity. In Table 1 we present data for the key parameters to fit the data. In our model we have two CIGS
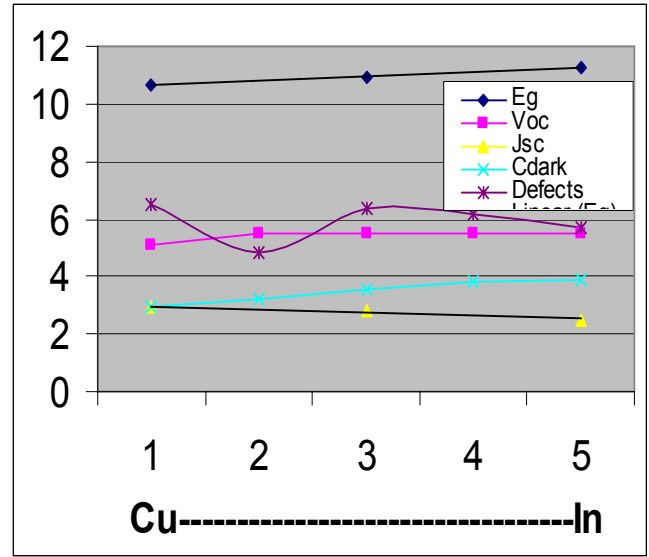

Figure 3. Plot of various parameters vs. Cu/In composition.

Eg	Voc	Jsc	Acceptor Density		Acceptor Defect Density	
			n	i	n	i
1.05	450	32.5	1e16	1e16	1e18	1e16
1.15	550	23.3	1.7e16	1.7e16	2.5e18	2.5e16

Table 1. AMPS parameters used to simulate device data.

layers, a top "n" layer that is about 100 nm thick and an "i" layer that is about 2 microns thick. As can be seen, we had to increase acceptor concentration and acceptor defect density together in both layers to match the observed data that accompany band gap changes. This is reminiscent of defect pairs often referred to in the literature. In fact, the acceptor defect in our AMPS simulation is located 0.29 eV above the valence band as designated by the NREL theory group for the V_{Cu}[1]. Thus V_{Cu} / Ga pairs seem to be responsible for the acceptor/acceptor defect pairing needed for successful simulation. The acceptor defect density in the n layer is the highest due to the proximity of that region to the top interface with CdS/ZnO. Controlling the defect density in this region is key to improving Voc's. Also, the proportional increase in defects is higher than acceptors for the higher band gap. This indicates that in this case the complex formed by ecxess Ga and In produces a defect and 1.5 acceptors. Additional experiments are under way to further our understanding of these phenomena. Meanwhile we have used these insights to move our Jsc's up to the ideal curve as shown by the experimental data point( ) at 1.09 eV in figure 1.

3.   **References**

1. Su-Huai Wei, S. B. Zhang, and Alex Zunger, *Appl. Phys. Lett*., **72**(4), 3199 (1998).